

# Intrinsic Threshold Voltage Fluctuations in Decanano MOSFETs Due to Local Oxide Thickness Variations

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**Abstract**—Intrinsic threshold voltage fluctuations introduced by local oxide thickness variations (OTVs) in deep submicrometer (decanano) MOSFETs are studied using three-dimensional (3-D) numerical simulations on a statistical scale. Quantum mechanical effects are included in the simulations employing the density gradient (DG) formalism. The random Si/SiO<sub>2</sub> and gate/SiO<sub>2</sub> interfaces are generated from a power spectrum corresponding to the autocorrelation function of the interface roughness. The impact on the intrinsic threshold voltage fluctuations of both the parameters used to reconstruct the random interface and the MOSFET design parameters are studied using carefully designed simulation experiments. The simulations show that intrinsic threshold voltage fluctuations induced by local OTV become significant when the dimensions of the devices become comparable to the correlation length of the interface. In MOSFETs with characteristic dimensions below 30 nm and conventional architecture, they are comparable to the threshold voltage fluctuations introduced by random discrete dopants.

**Index Terms**—MOSFETs, numerical simulation, oxide thickness fluctuation, quantum effects, 3-D threshold.

## I. INTRODUCTION

THE scaling of the MOSFET to decanano (sub-50-nm) dimensions near the end of the International Technology Roadmap for Semiconductors [1] involves aggressive reduction in the gate oxide thickness [2]. Prototype MOSFETs with conventional architecture, gate length of 30 nm, and oxide thickness below 10 Å have already been successfully demonstrated [3]. In such devices, not only the discrete and random dopant charge [4]–[6], but also the atomic scale roughness of the Si/SiO<sub>2</sub> and gate/SiO<sub>2</sub> interfaces will introduce significant intrinsic parameter fluctuations. Indeed, when the oxide thickness is equivalent to only a few silicon atomic layers, the atomic scale interface roughness steps [7] will result in significant oxide thickness variation (OTV) within the gate region of an individual MOSFET. The unique random pattern of the gate oxide thickness and interface landscape makes each decanano MOSFET different from its counterparts and leads to variations in the surface roughness limited mobility, gate tunnelling current [8], [9], and real [10] or apparent threshold voltage [11] from device to device.

Similar to the simulation of random dopant fluctuation effects [12], the numerical study of local oxide thickness fluctuation effects requires three-dimensional (3-D) statistical simulations of ensembles of MOSFETs with macroscopically identical design parameters but with microscopically different oxide thickness/interface patterns. It is also important to include quantum mechanical confinement effects [13], which push the inversion layer away from the rough interface and smooth the spatial inversion charge variations [14] compared to classical simulations.

In this paper, we use 3-D numerical simulations on a statistical scale to investigate intrinsic threshold voltage fluctuations induced by random local OTV in decanano MOSFETs with gate oxide thickness in the range 1–3 nm. We demonstrate the importance of this phenomenon in carefully designed simulation examples, and explore the extent of its impact on the next generation decanano MOSFETs. Quantum mechanical corrections are included in the simulations using the density gradient (DG) formalism [14], [15]. At this stage, the simulations reflect the electrostatic effects associated with the OTVs, but do not include variation in the interface-roughness limited mobility and the gate tunnelling current.

Section II describes in detail our simulation approach. After a brief introduction of the simulator itself, we give details about the generation of the random oxide interface. The importance of the quantum corrections introduced using the DG algorithm is also illustrated in a specifically designed simulation experiment. The results of the systematic simulation study are presented and discussed in Section III. They highlight both the impact of the parameters used to generate the random interface and the device design parameters on the intrinsic threshold voltage fluctuations induced by random OTVs. The scale of this phenomenon is compared with the random dopant induced threshold voltage fluctuations in identical devices. The conclusions are drawn in section IV.

## II. SIMULATION APPROACH

The results presented in this paper are obtained using a hierarchical 3-D drift-diffusion simulator [12] with DG quantum corrections [15], originally designed for studying random dopant fluctuation effects in decanano MOSFETs. Bearing in mind that, depending on the silicon substrate orientation [7], the interface roughness steps are on the scale of 0.2–0.3 nm, the proper resolution of the OTV effects in the simulation of individual MOSFETs require a 3-D solution with very fine discretization near the interface. Continuous doping charge is used in most of the simulations instead of random

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discrete dopants in order to isolate the threshold voltage fluctuation effects associated with OTV. The requirement for statistical analysis and interpretation of the results transforms the problem effectively into a four-dimensional one, where the fourth dimension is the size of the statistical sample of devices with identical design parameters but microscopically different pattern of gate oxide thickness/interface. Statistical samples of 200 MOSFETs are simulated and analyzed for each combination of device design and interface roughness parameters producing typically one data point on the graphs, which will be presented later. In order to save computational time in the laborious statistical simulation experiments, similar to [15], the simulations are restricted to low drain voltage. Current criterion  $I_T = 10^{-8} W_{\text{eff}}/L_{\text{eff}} [A]$ , where  $W_{\text{eff}}$  and  $L_{\text{eff}}$  are the effective channel width and length, respectively, is used to estimate the threshold voltage of an individual device. Since the threshold voltage is extracted in the subthreshold region, where the current depends exponentially on the gate voltage, the choice of the mobility model has a negligible effect on the accuracy of the presented results.

#### A. Modeling the Interface

The exact details of the Si/SiO<sub>2</sub> interface are still the subject of intensive research despite a constant interest from industry and academe over the last couple of decades. Some of the difficulties in the past stemmed from employing transmission electron microscopy (TEM) which is a two-dimensional (2-D) projection technique to study an inherently 3-D and chemically incoherent interface [16], [17]. In addition, sensitivity to the ambient conditions during fabrication, and to the material quality on either side of the interface, can often create further complications. However, the significant advance during the last decade in ultra-high-resolution analytic techniques, including atomic force microscopy (AFM) [18], scanning reflection electron microscopy (SREM) [19], surface second harmonic generation, and X-ray scattering analysis [20], has advanced significantly the understanding of the Si/SiO<sub>2</sub> interface.

The random 2-D surfaces used to represent the boundary between the oxide and the silicon and/or between the oxide and the gate material in our simulation are constructed using standard assumptions for the auto-correlation function of the interface roughness. Generally, the interface is described by a Gaussian or exponential auto-correlation function with a given correlation length  $\Lambda$  and rms height  $\Delta$  [17]. The corresponding power spectrum can be obtained by 2-D Fourier transformation (in radial coordinates). In order to reconstruct the interface, we generate in the Fourier domain a complex  $N \times N$  matrix. The magnitude of the elements of this matrix follows the power spectrum of the chosen correlation function, while the phase is selected at random. Several conditions [21] must be satisfied to ensure that the corresponding 2-D surface in real space, obtained by inverse Fourier transformation, represents a real function. The “analog” random 2-D surface obtained using this procedure is then quantized in steps to take into account the discrete nature of the interface roughness steps associated with the atomic layers in the crystalline silicon substrate [7]. The step height is approximately 0.3 nm for the (001) interface.

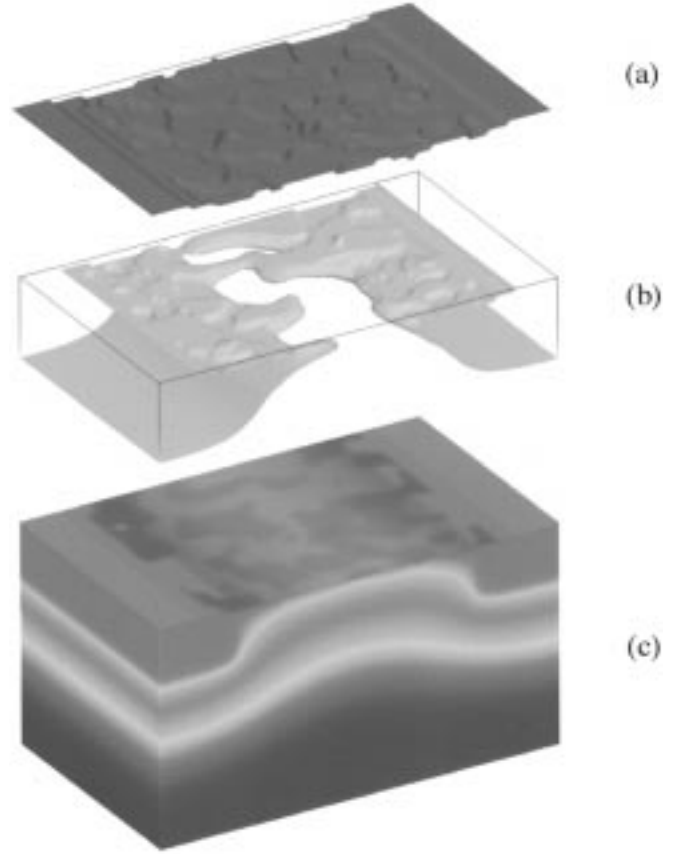


Fig. 1. (a) Typical profile of the random Si/SiO<sub>2</sub> interface in a  $30 \times 30 \text{ nm}^2$  MOSFET, followed by (b) an equiconcentration contour obtained from DG simulations, and (c) the potential distribution.

A typical random Si/SiO<sub>2</sub> interface, generated according to the above described procedure and used in the simulation of a  $30 \times 30 \text{ nm}^2$  MOSFET described in detail in Section III, is shown at the top of Fig. 1. The interface has been reconstructed using a power spectrum corresponding to a Gaussian correlation function. Only the roughness of the Si/SiO<sub>2</sub> interface was introduced in the simulations and the gate/SiO<sub>2</sub> interface was flat. The potential distribution at threshold voltage is shown at the bottom of Fig. 1. The oxide thickness fluctuations introduce surface potential fluctuations similar to the fluctuations introduced by random impurities. DG quantum corrections are included in the simulation. One equiconcentration surface corresponding to electron charge density  $1 \times 10^{17} \text{ cm}^{-3}$  is plotted in the middle, illustrating the quantum confinement effects in both vertical and lateral directions.

#### B. Quantum Mechanical Effects

As described in [15], the DG quantum corrections have been carefully calibrated in the direction normal to the channel against rigorous one-dimensional (1-D) full-band Poisson–Schrödinger simulations [13]. Excellent agreement has been achieved both in terms of threshold voltage shift and inversion layer charge distribution. It has been also demonstrated in 2-D examples [14] that DG simulations give a qualitatively correct result in respect to lateral confinement effects associated with the roughness of the Si/SiO<sub>2</sub> interface. However, the rigorous

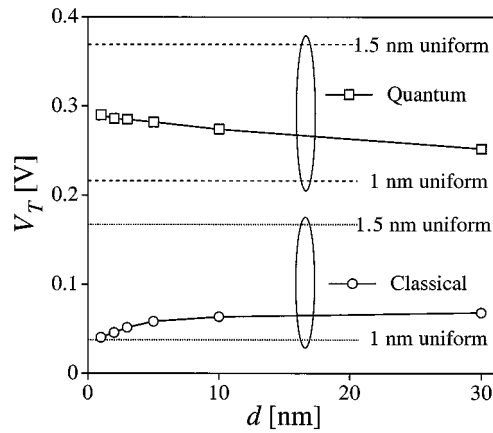


Fig. 2. Threshold voltage of a  $30 \times 30 \text{ nm}^2$  MOSFET as a function of the period  $d$  of the variations in the oxide thickness at the Si/SiO<sub>2</sub> interface. The thick (1.5 nm) and the thin (1 nm) oxide strips are aligned with the direction of the current flow in the channel. Results from classical and DG simulations are compared.

calibration of the DG simulations in respect to quantum confinement in the plane of the channel is still an open issue.

In order to illustrate the importance of quantum confinement when studying OTV effects, simulation experiments were carried out in a  $30 \times 30 \text{ nm}^2$  MOSFET with periodical gate oxide structure with alternating thin (1 nm) and thick (1.5 nm) oxide strips in the direction parallel to the current flow in the channel. The dependence of the threshold voltage on the period  $d$  of the gate stripes, calculated classically and with DG quantum corrections, is illustrated in Fig. 2. Completely opposite trends are observed in the two sets of simulations. The classical results show reduction in the threshold voltage as  $d$  decreases, while the quantum mechanical results show an increase in the threshold voltage.

The explanation of the opposite trends becomes apparent in Fig. 3. The top of the figure illustrates the Si/SiO<sub>2</sub> interface followed by two equiconcentration surfaces obtained from classical and DG simulations. The bottom of the figure illustrates the potential distribution. In the classical simulations, there is an increase in the carrier concentration at the corners of the inverted silicon wells due to field crowding there. Such field crowding is responsible, for example, for the inverse narrow channel effect observed in MOSFETs with shallow trench isolation [22]. The increasing numbers of high current density contributions from the corners, when the period of the stripes decreases, results in a reduction of the threshold voltage in the classical case. However, due to 2-D confinement effects, the quantum mechanical charge distribution cannot follow the local increase in the potential in the corners and the maximum in the charge distribution moves to the middle of the wells, resulting in an effective narrowing of the current filaments. This is causing an increase in the threshold voltage when  $d$  becomes smaller.

Similar 2-D confinement effects, pushing the maximum of the inversion charge distribution to the middle of the current filaments formed by the random pattern of the interface roughness, are noticeable in the equiconcentration contour shown in Fig. 1. In this case, the height of the interface roughness steps responsible for the lateral confinement is only 0.3 nm.

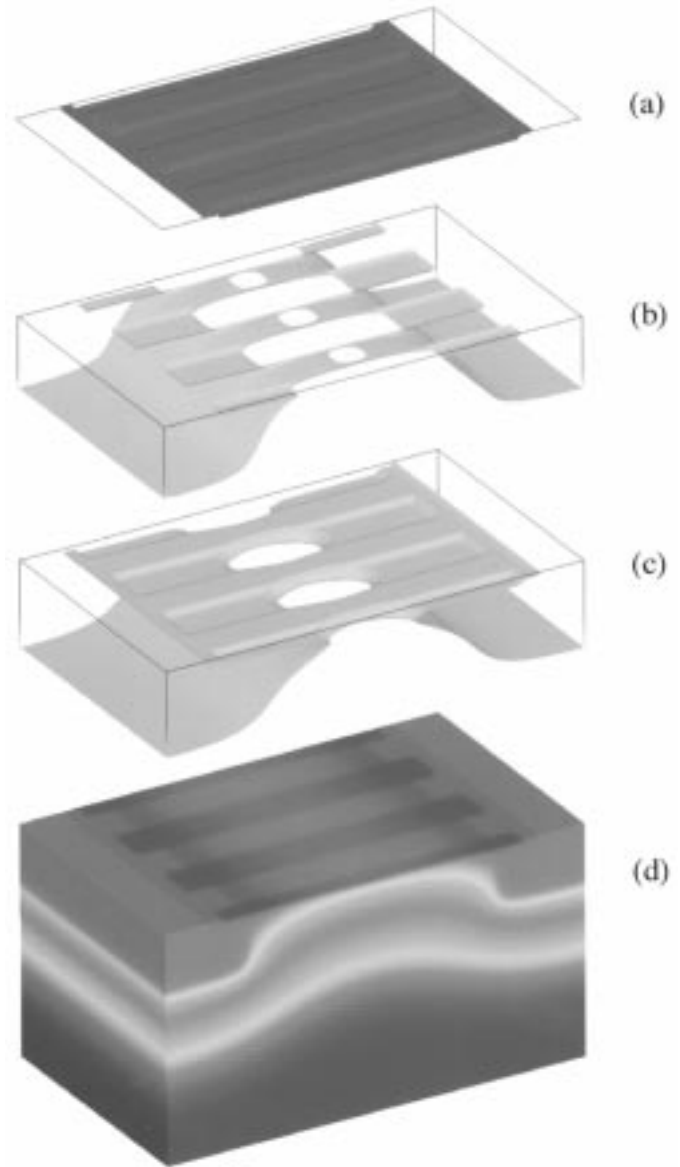


Fig. 3. (a) Profile of the Si/SiO<sub>2</sub> interface in a  $30 \times 30 \text{ nm}^2$  gate oxide “superlattice” MOSFET, followed by two equiconcentration surfaces obtained from (b) classical and (c) DG simulations, and (d) the potential distribution.

### III. RESULTS AND DISCUSSION

The generic device simulated in this study is an  $n$ -channel  $30 \times 30 \text{ nm}^2$  MOSFET with simplified, but well-scaled, architecture. The typical average oxide thickness  $\langle t_{\text{ox}} \rangle$  is 1.05 nm. The junction depth  $x_j$  is 7 nm. The acceptor doping concentration  $N_A$ , which is constant in the channel region, is  $5 \times 10^{18} \text{ cm}^{-3}$ . Continuous doping distribution instead of random discrete dopants is used in most of the simulations. In the simulation experiments, one design parameter is typically varied while the rest remain as specified above. The polysilicon depletion effects are excluded and the gate potential is fixed at the gate/SiO<sub>2</sub> interface.

The choice of autocorrelation function and the corresponding power spectrum when generating the random interface is controversial. Early attempts to fit surface roughness limited mobility

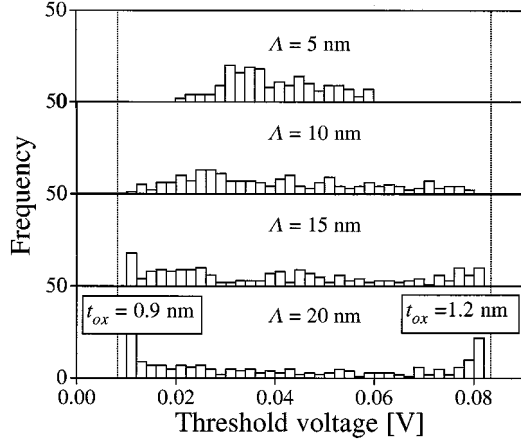


Fig. 4. Threshold voltage variation in a  $30 \times 30 \text{ nm}^2$  MOSFET with average oxide thickness  $\langle t_{\text{ox}} \rangle = 1.05 \text{ nm}$  for different correlation lengths of the Gaussian power spectrum used to generate the Si/SiO<sub>2</sub> interface.

to experimental data were used a Gaussian autocorrelation function [23]. Later, the preference changed to an exponential one [17]. The most recent studies show that both Gaussian and exponential autocorrelation functions can fit the experimental mobility data but need different parameters for electrons and holes [24]. It was also demonstrated in [24] that electron and hole mobility data could be fitted using identical parameters, if a power spectrum, which has a Gaussian shape for small wave vector exchange  $q$  but a steeper decay for large  $q$ , is used. In this paper, we have adopted a Gaussian power spectrum for generating the random interface. The corresponding 2-D surface is smoother compared to the one generated using an exponential autocorrelation function and less demanding from a grid generation point of view.

#### A. Correlation Length Dependence

There is a relatively close agreement in the rms values,  $\Delta$ , of the interface roughness reported by different sources. In the same time there is more than one order of magnitude difference in the reported values for the correlation length  $\Lambda$ . Correlation lengths in the range of 1–3 nm are reported from TEM measurements [17] and are typically used to fit surface roughness limited mobility to experimental data [24]–[26]. At the same time, the values of  $\Lambda$  reported from AFM measurements vary from 10 to 30 nm [18], [26]. Bearing in mind this uncertainty, we first study the impact of  $\Lambda$  on the threshold voltage variation.

The threshold voltage variation in the generic  $30 \times 30 \text{ nm}^2$  MOSFET is illustrated in Fig. 4 for different values of  $\Lambda$ . Only roughness at the Si/SiO<sub>2</sub> interface is considered in this case. The sample size in all histograms is 200. The average oxide thickness  $\langle t_{\text{ox}} \rangle$  is 1.05 nm. The interface roughness is quantized allowing only one step of 0.3 nm, which results in the generation of random oxide regions with thickness 0.9 nm and 1.2 nm, respectively. For small values of  $\Lambda$ , the distribution of the threshold voltage is close to a Gaussian. With the increase of  $\Lambda$  a broadening of the distribution occurs. When  $\Lambda$  becomes comparable with the characteristic dimensions of the MOSFET, two peaks corresponding to the 0.9 nm and 1.2 nm oxide thickness become apparent. It is clear that, for correlation lengths

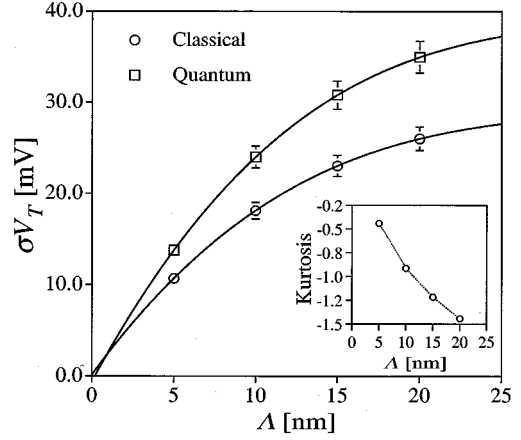


Fig. 5. Dependence of the threshold voltage standard deviation  $\sigma V_T$  on the correlation length  $\Lambda$  for the  $30 \times 30 \text{ nm}^2$  MOSFETs as in Fig. 4. Classical and DG simulation results are compared.

much larger than the characteristic device dimension, there is a high probability that in the whole gate region the oxide will be either 0.9 nm or 1.2 nm thick and most of the devices will have the corresponding uniform oxide threshold voltages. There will be, however, threshold voltages in between associated with MOSFETs in which a boundary between thin and thick oxide regions divides the channel along the direction of the current flow.

The dependence of the threshold voltage standard deviation  $\sigma V_T$  on  $\Lambda$  obtained from classical and DG simulations is compared in Fig. 5. The introduction of quantum corrections results in an increase in the threshold voltage variation. We believe that this is related to the lateral confinement effects, which narrow the current percolation paths. In both cases, the dependence of  $\sigma V_T$  on  $\Lambda$  is linear for correlation lengths much smaller than the characteristic MOSFET dimensions and saturates for large  $\Lambda$ . The dependence of the kurtosis as a function of  $\Lambda$  in the DG case is shown in the inset of the same figure. The increasingly negative values of the kurtosis are indication for the flattening of the  $V_T$  distribution with the increase of the correlation length.

The shape of the  $\sigma V_T$  dependence on  $\Lambda$  can be easily understood qualitatively. The binary distribution of the threshold voltage at  $\Lambda \gg L_{\text{eff}}, W_{\text{eff}}$  result in  $\sigma V_T$  saturation at a value  $\sigma V_T^{\text{max}} \approx (V_T(t_{\text{ox}} = 12 \text{ \AA}) - V_T(t_{\text{ox}} = 9 \text{ \AA}))/2$ . This gives, for example,  $\sigma V_T^{\text{max}} = 49 \text{ mV}$  in the DG case. In the case where  $\Lambda \ll L_{\text{eff}}, W_{\text{eff}}$ , we assume as a simplification that gate area  $W_{\text{eff}} \times L_{\text{eff}}$  is divided into uniform  $\Lambda/2$ -sided squares, each with thin or thick oxide at random. Averaging the contribution of a total of  $N$  cells, where  $N = 4W_{\text{eff}}L_{\text{eff}}/\Lambda^2$ , the standard deviation of threshold is reduced by a factor of  $\sqrt{N}$ . Therefore

$$\sigma V_T = \frac{\Lambda \sigma V_T^{\text{max}}}{2\sqrt{W_{\text{eff}}L_{\text{eff}}}}. \quad (1)$$

Thus, for very small values of  $\Lambda$ , the standard deviation should increase linearly.

Bearing in mind the strong dependence of  $\sigma V_T$  on  $\Lambda$ , and the uncertainties in this parameter, we have carried out further investigations for two characteristic correlation lengths. The first

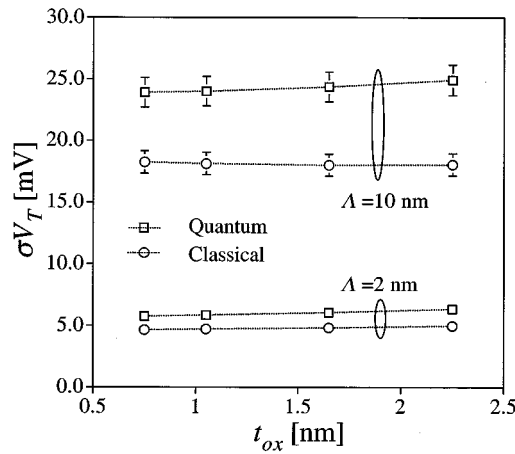


Fig. 6. Dependence of threshold voltage standard deviation  $\sigma V_T$  on the average oxide thickness  $\langle t_{ox} \rangle$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with random Si/SiO<sub>2</sub> interface.

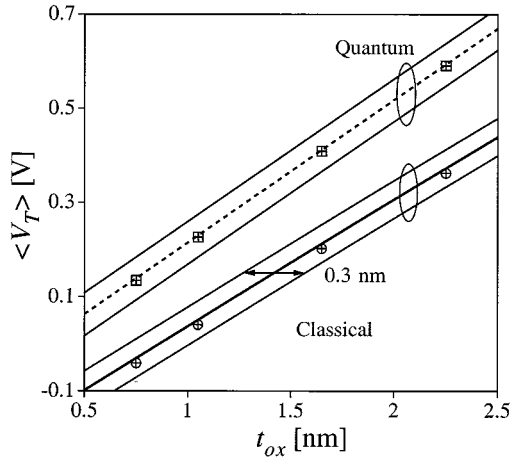


Fig. 7. Dependence of the average threshold voltage  $\langle V_T \rangle$  on the average oxide thickness  $\langle t_{ox} \rangle$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with random Si/SiO<sub>2</sub> interface (symbols) and of the threshold voltage  $V_T$  on the oxide thickness  $t_{ox}$  for a similar device with uniform oxide (lines).

one,  $\Lambda = 2 \text{ nm}$ , is in the middle of the values used to fit mobility data. The second one,  $\Lambda = 10 \text{ nm}$ , is at the lower end of correlation lengths extracted from AFM measurements, but for the  $30 \times 30 \text{ nm}^2$  MOSFETs gives a distribution which is not strongly peaked at the two bounding values of  $V_T$ .

### B. Oxide Thickness (*In*)dependence

The dependence, or more accurately the virtual independence, of  $\sigma V_T$  on the average oxide thickness  $\langle t_{ox} \rangle$  for a  $30 \times 30 \text{ nm}^2$  MOSFET is illustrated in Fig. 6. Again, roughness only at the Si/SiO<sub>2</sub> interface is considered in the simulations. This trend is related to the linear dependence between  $V_T$  and  $t_{ox}$  known from the textbook expression for the threshold voltage, which results in a constant variance in respect to oxide thickness. We also present in Fig. 7 the dependence of the average threshold voltage  $\langle V_T \rangle$  on  $\langle t_{ox} \rangle$  calculated classically and quantum mechanically, this time only for  $\Lambda = 10 \text{ nm}$  (symbols). For comparison, the dependence of the threshold voltage  $V_T$  of devices with uniform oxide thickness

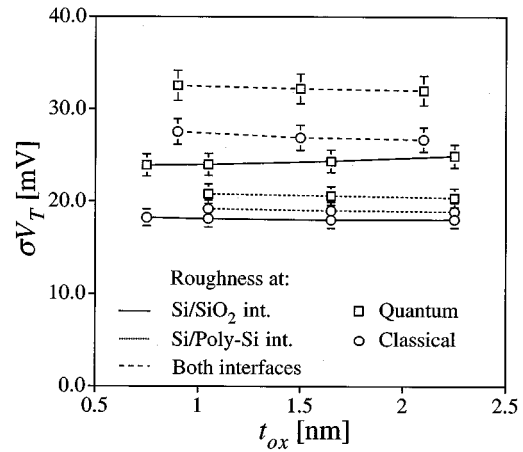


Fig. 8. Dependence of threshold voltage standard deviation  $\sigma V_T$  on the average oxide thickness  $\langle t_{ox} \rangle$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with roughness at the Si/SiO<sub>2</sub> interface, at the gate Si/SiO<sub>2</sub> interface, and at both interfaces  $\Lambda = 10 \text{ nm}$  in all cases.

$t_{ox}$  is plotted in the same figure as a function of  $t_{ox}$  (lines). It is clear that the average threshold voltage  $\langle V_T \rangle$  of the devices with random oxide thickness is very close to the corresponding threshold voltage of uniform oxide MOSFETs with  $t_{ox} = \langle t_{ox} \rangle$ . The slight lowering of  $\langle V_T \rangle$  in the classical case is associated with the increase of the current density at the boundaries between the thinner and thicker oxide regions due to the field crowding effect discussed in Section II.B.

Although very little is known about the properties and the description of the gate/SiO<sub>2</sub> interface, we have designed simulation experiments in an attempt to understand its importance for the threshold voltage variation. The graphs presented in Fig. 8 summarize the results of these experiments in which only one correlation length  $\Lambda = 10 \text{ nm}$  is considered. In the first experiment, roughness was introduced at the gate/SiO<sub>2</sub> and the Si/SiO<sub>2</sub> interface was flat. The parameters used to generate the random gate/SiO<sub>2</sub> interface were identical to the parameters used previously to generate the Si/SiO<sub>2</sub> interface. In the classical simulations, the amount of threshold voltage fluctuations introduced by roughness at the top and at the bottom interfaces is the same. In the DG simulations, the roughness at the top interface results in smaller  $\sigma V_T$  compared to roughness at the bottom interface. This is consistent with the assumption made in Section III. A that the quantum enhancement in the threshold voltage fluctuations is related to lateral confinement effects. In this case, the lateral confinement is weaker resulting only from potential fluctuations introduced at the smooth Si/SiO<sub>2</sub> interface by the rough gate/SiO<sub>2</sub> interface. In the second simulation experiment, uncorrelated roughness was introduced at both interfaces. The analysis shows that the threshold voltage fluctuations introduced by each of the interfaces are statistically independent, and the total threshold voltage standard deviation in this case closely follows the relationship  $\sigma V_T^{\text{tot}} = \sqrt{(\sigma V_T^{\text{top}})^2 + (\sigma V_T^{\text{bottom}})^2}$ . To the best of our knowledge, there are no conclusive measurements and agreement in the literature to what extent the roughness at the channel and the gate interfaces are uncorrelated. The question

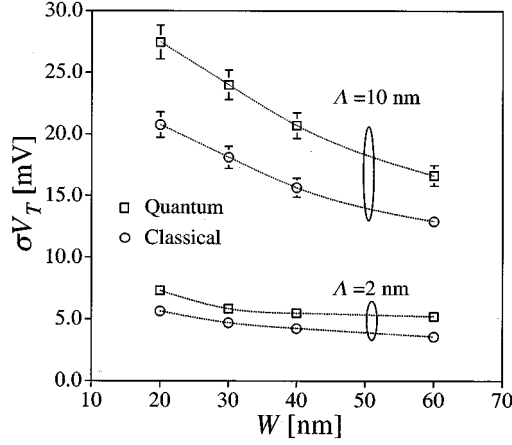


Fig. 9. Dependence of threshold voltage standard deviation  $\sigma V_T$  on effective channel width  $W_{\text{eff}}$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with random Si/SiO<sub>2</sub> interface.

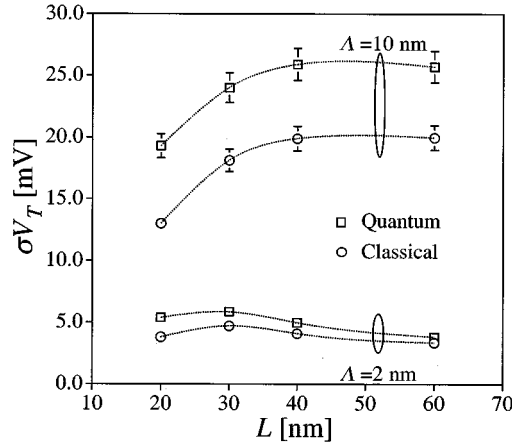


Fig. 10. Dependence of threshold voltage standard deviation  $\sigma V_T$  on the effective channel length  $L_{\text{eff}}$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with random Si/SiO<sub>2</sub> interface.

“What will happen if the roughness at the both interfaces is due to steps in the original silicon surface and therefore strongly correlated?” will be addressed in a follow-up paper.

### C. Geometry Dependence

The dependence of  $\sigma V_T$  on the effective channel width  $W_{\text{eff}}$  and the effective channel length  $L_{\text{eff}}$  are illustrated in Figs. 9 and 10, respectively. The variation of  $\sigma V_T$  in respect to  $W_{\text{eff}}$  follows closely the expected  $1/\sqrt{W_{\text{eff}}}$  dependence from (1). The variation of  $\sigma V_T$  in respect to  $L_{\text{eff}}$  follows the  $1/\sqrt{L_{\text{eff}}}$  dependence only for  $\Lambda = 2 \text{ nm}$  and for values of  $L_{\text{eff}}$  larger than 30 nm. For  $L_{\text{eff}} < 30 \text{ nm}$  2-D charge sharing effects significantly reduce the amount of the charge in the channel controlled by the gate and its contribution to the threshold voltage variation, which results in a departure from the  $1/\sqrt{L_{\text{eff}}}$  dependence. This effect is more pronounced at correlation length  $\Lambda = 10 \text{ nm}$  where the departure from the  $1/\sqrt{L_{\text{eff}}}$  dependence of  $\sigma V_T$  occurs at effective channel lengths below 40 nm.

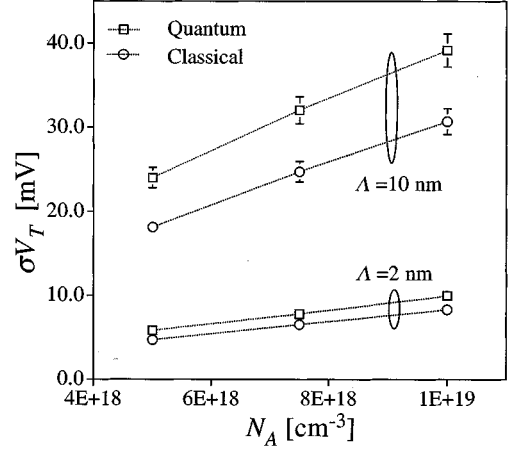


Fig. 11. Dependence of threshold voltage standard deviation  $\sigma V_T$  on the channel doping concentration  $N_A$  for a  $30 \times 30 \text{ nm}^2$  MOSFET with random Si/SiO<sub>2</sub> interface.

### D. Doping Concentration Dependence

Doping concentration  $N_A$  higher than  $5 \times 10^{18} \text{ cm}^{-3}$  will be required to suppress short-channel effects and to adjust the threshold when the conventional MOSFET is scaled to channel lengths below 30 nm. As shown in Fig. 11, the standard deviation of the threshold voltage  $\sigma V_T$  in the  $30 \times 30 \text{ nm}^2$  MOSFET increases sublinearly with the increase in the doping concentration following a dependence stronger than  $\sqrt{N_A}$ .

The results from Fig. 11 obtained with DG quantum corrections serve in Fig. 12 as a basis for comparing the standard deviation in the threshold voltage induced by OTV  $\sigma V_T^{\text{OTV}}$  and the standard deviation in the threshold voltage induced by dopant fluctuations  $\sigma V_T^{\text{DF}}$ . In order to isolate the doping fluctuation (DF) effects, simulations were carried out first using random discrete dopants and uniform gate oxide. The corresponding  $\sigma V_T^{\text{DF}}$  is approximately two times larger than  $\sigma V_T^{\text{OTV}}$  for correlation length  $\Lambda = 10 \text{ nm}$ , and more than five times larger for  $\Lambda = 2 \text{ nm}$ . However, with the increase in the doping concentration, the gap between  $\sigma V_T^{\text{DF}}$  and  $\sigma V_T^{\text{OTV}}$  closes up. Referring back to Figs. 5 and 8, it is clear that for correlation lengths larger than 10 nm, taking into account the roughness at both interfaces, the intrinsic parameter variations associated with OTV and dopant fluctuations become comparable.

Finally, simulations were carried out in which the OTV and the dopant fluctuations are taken into account simultaneously. The close inspection of the results reveals that the two sources of intrinsic parameter fluctuations act in a statistically independent manner resulting in a total standard deviation  $\sigma V_T^{\text{tot}}$  which closely follows the relationship  $\sigma V_T^{\text{tot}} = \sqrt{(\sigma V_T^{\text{OTV}})^2 + (\sigma V_T^{\text{DF}})^2}$ .

## IV. CONCLUSION

The interface roughness related oxide thickness fluctuations will introduce significant intrinsic fluctuation in the threshold voltage when the correlation length of the interface becomes comparable to the characteristic dimensions of aggressively

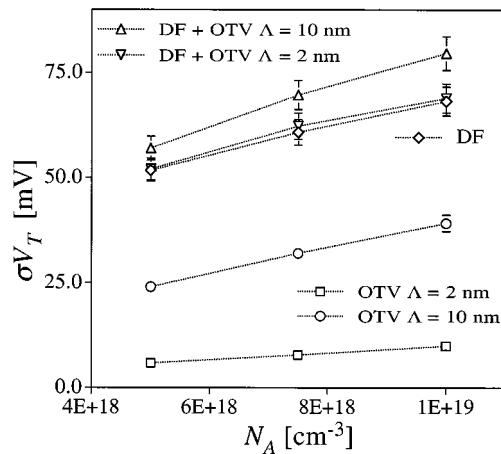


Fig. 12. Comparison of the standard deviation of the threshold voltage introduced by oxide thickness variation (OTV) and by doping fluctuations (DFs).

scaled MOSFETs near the end of the International Roadmap for Semiconductors. The introduction of quantum corrections in the simulations results in further increase of the fluctuations. In the oxide thickness range of 1–3 nm, the intrinsic threshold voltage fluctuations are practically independent of the oxide thickness. The fluctuations introduced by uncorrelated Si/SiO<sub>2</sub> and the gate/SiO<sub>2</sub> interfaces are statistically independent. A departure from the expected  $1/\sqrt{\text{Area}}$  dependence of the threshold voltage standard deviation is observed when the short-channel effects start to play a significant role. The doping concentration dependence of the threshold voltage standard deviation is sublinear but stronger than  $\sqrt{N_A}$ . For devices with characteristic dimensions below 30 nm, the oxide thickness induced threshold voltage fluctuations become comparable to the fluctuations induced by random discrete dopants, particularly when the contribution of both interfaces is taken into account and the larger correlation length suggested by AFM measurements are adopted.

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#### REFERENCES

- [1] *The International Technology Roadmap for Semiconductors*. 1999 Edition.
- [2] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Sato, and H. Iwai, "1.5-nm direct-tunnelling gate oxide Si MOSFETs," *IEEE Trans. Electron Devices*, vol. 43, pp. 1233–1241, June 1996.
- [3] R. Chau, J. Kabalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murty, and G. Dewey, "30-nm physical gate length CMOS transistor with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays," in *IEDM Tech. Dig.*, 2001, pp. 45–48.
- [4] R. W. Keys, "Physical limits in digital electronics," *Proc. IEEE*, vol. 63, pp. 740–766, Feb. 1975.
- [5] H.-S. Wong and Y. Taur, "Three-dimensional "atomistic" simulation of discrete random dopant distribution effects in sub-0.1- $\mu$ m MOSFETs," in *IEDM Tech. Dig.*, 1993, pp. 705–708.
- [6] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1- $\mu$ m MOSFETs: A 3-D "atomistic" simulation study," *IEEE Trans. Electron Devices*, vol. 45, pp. 2505–2513, Dec. 1998.
- [7] M. Niva, T. Kouzaki, K. Okada, M. Udagawa, and R. Sinclair, "Atomic-order planarization of ultrathin SiO<sub>2</sub>/Si(001) interface," *Jpn. J. Appl. Phys.*, vol. 33, pp. 388–394, 1994.
- [8] D. Z.-Y. Ting, E. S. Daniel, and T. C. McGill, "Interface roughness effects in ultrathin gate oxides," *VLSI Syst. Des.*, vol. 8, pp. 47–51, 1998.
- [9] E. Cassan, P. Dollfus, S. Galdin, and P. Hesto, "Calculation of direct tunnelling gate current through ultrathin oxide and oxide/nitride stacks in MOSFETs and H-MOSFETs," *Microelectron. Reliab.*, vol. 40, pp. 585–588, 2000.
- [10] A. Asenov and S. Kaya, "Effect of oxide roughness on the threshold voltage fluctuations in decanano MOSFETs with ultrathin gate oxide," in *Proc. SISPAD*, 2000, pp. 135–138.
- [11] M. Koh, W. Mizubayashi, K. Ivamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, and M. Hirose, "Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation introduced by tunnelling leakage current," *IEEE Trans. Electron Devices*, vol. 48, pp. 259–264, Jan. 2001.
- [12] A. Asenov, A. R. Brown, J. H. Davies, and S. Saini, "Hierarchical approach to "atomistic" 3-D MOSFET simulation," *IEEE Trans. Computer-Aided Design*, vol. 18, pp. 1558–1565, Dec. 1999.
- [13] S. Jallepalli, J. Bude, W.-K. Shih, M. R. Pinto, C. M. Maziar, and A. F. Tasch Jr., "Electron and hole quantization and their impact on deep submicrometer silicon p- and n-MOSFET characteristics," *IEEE Trans. Electron Devices*, vol. 44, pp. 297–303, Feb. 1997.
- [14] C. S. Rafferty, B. Biegel, Z. Yu, M. G. Ancona, J. Bude, and R. W. Dutton, "Multi-dimensional quantum effects simulation using a density-gradient model and script-level programming technique," in *Proc. SISPAD*, K. De Meyer and S. Biesemans, Eds., 1998, pp. 137–140.
- [15] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100-nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study," *IEEE Trans. Electron Devices*, vol. 48, pp. 722–729, Apr. 2001.
- [16] P. O. Hahn and M. Henzler, "The Si-SiO<sub>2</sub> interface: Correlation of atomic structure and electrical properties," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 2, pp. 574–583, 1984.
- [17] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the Si(100)-SiO<sub>2</sub> interface," *Phys. Rev. B, Condens. Matter*, vol. 32, pp. 8171–8186, 1985.
- [18] T. Yoshinobu, A. Ivamoto, and H. Iwasaki, "Scaling analysis of SiO<sub>2</sub>/Si interface roughness by atomic force microscopy," *Jpn. J. Appl. Phys.*, vol. 33, pp. 383–387, 1994.
- [19] N. Miyata, H. Watanabe, and M. Ichikawa, "HF-chemical etching of the oxide layer near SiO<sub>2</sub>/Si(111) interface," *Appl. Phys. Lett.*, vol. 73, pp. 3923–3925, 1998.
- [20] S. T. Cundiff, W. H. Knox, and F. H. Baumann, "Si/SiO<sub>2</sub> interface roughness: Comparison surface second harmonic generation and X-ray scattering," *Appl. Phys. Lett.*, vol. 70, pp. 1414–1416, 1997.
- [21] R. M. Feenstra, M. A. Lutz, F. Stern, K. Ismail, P. M. Mooney, F. K. LeGoues, C. Stanis, J. O. Chu, and B. S. Meyerson, "Roughness analysis of Si/SiGe heterostructures," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 13, pp. 1608–1612, 1995.
- [22] S.-C. Lin, J. B. Kuo, K.-T. Huang, and S.-W. Sun, "A closed-form back gate bias related inverse narrow channel effect model for deep submicrometer VLSI CMOS devices using shallow trench isolation," *IEEE Trans. Electron Devices*, vol. 47, pp. 725–733, Apr. 2000.
- [23] R. E. Prange and T. W. Nee, "Quantum spectroscopy of the low field oscillations in the surface impedance," *Phys. Rev.*, vol. 168, pp. 779–786, 1968.
- [24] A. Pirovano, A. L. Lacaita, G. Zandler, and R. Oberhuber, "Explaining the dependence of the hole and electron mobilities in Si inversion layers," *IEEE Trans. Electron Devices*, vol. 47, pp. 718–724, Apr. 2000.
- [25] S. Yamakawa, H. Ueno, K. Taniguchi, C. Hamaguchi, K. Masali, and U. Ravioli, "Study of interface roughness dependence of electron mobility in Si inversion layers using Monte Carlo method," *J. Appl. Phys.*, vol. 79, pp. 911–916, 1996.
- [26] A. Pirovano, A. L. Lacaita, G. Gidini, and G. Talarida, "On the correlation between surface roughness and inversion layer mobility in Si-MOSFETs," *IEEE Electron Device Lett.*, vol. 21, pp. 34–36, Jan. 2000.



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